IN THE CLAIMS

Please cancel claims 7-39 without prejudice.

Please amend claim 3 as follows below.

Please add new claims 40-51 as follow below.

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Marked Up Listing of Claims:

1. (Original) A method to conserve power comprising:

in a digital signal processor integrated circuit including an internal memory, a reduced instruction set computing (RISC) processor and one or more digital signal processing (DSP) units,

selectively swapping activity between the RISC processor and the one or more DSP units;

selectively stopping the clocking of respective one or more DSP units; and

selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters.

2. (Original) The method of claim 1, wherein

the selective swapping activity between the RISC processor and the one or more DSP units includes

activating and inactivating bus drivers on data paths in the RISC processor and the one or more DSP units.

3. (Currently Amended) The method of claim 1, wherein

the selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all

other memory clusters includes

selecting a data flow path between the activated memory cluster and the RISC processor and the one or more DSP units to change state while maintaining the state on data flow paths between the inactivated memory clusters and the RISC processor and the one or more DSP units.

4. (Original) The method of claim 1, wherein the selective stopping the clocking of respective one or more DSP units is responsive to those one or more DSP units being inactive.

5. (Original) The method of claim 1, wherein the selective stopping the clocking of respective one or more DSP units is responsive to those one or more DSP units not executing an instruction.

6. (Original) The method of claim 1, wherein the selective activating one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

7-39. (Cancelled)

40. (New) The method of claim 2, wherein the selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters includes

selecting a data flow path between the activated memory cluster and the RISC processor and the one or more

DSP units to change state while maintaining the state on data flow paths between the inactivated memory clusters and the RISC processor and the one or more DSP units.

41. (New) The method of claim 40, wherein the selective stopping the clocking of respective one or more DSP units is responsive to those one or more DSP units not executing an instruction.

42. (New) The method of claim 40, wherein the selective activating one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

43. (New) A method to conserve power in a digital signal processor integrated circuit, the method comprising:

in an integrated circuit

selectively swapping activity between a reduced instruction set computing (RISC) processor and a plurality of digital signal processing (DSP) units;

selectively stopping the clocking of at least one of the plurality of DSP units; and

selectively activating one of a plurality of memory clusters in an internal memory and maintaining a state of other memory clusters.

44. (New) The method of claim 43, wherein the selective swapping activity between the RISC processor and the plurality of DSP units includes

activating and inactivating bus drivers on data paths in the RISC processor and the plurality of DSP units.

45. (New) The method of claim 43, wherein the selectively activating one of a plurality of memory clusters in the internal memory and maintaining a state of all other memory clusters includes

selecting a data flow path between the activated memory cluster and the RISC processor and the plurality of DSP units, the selected data flow path to change state while maintaining the state on data flow paths between inactivated memory clusters and the RISC processor and the plurality of DSP units.

46. (New) The method of claim 43, wherein the selective stopping the clocking of respective plurality of DSP units is responsive to at least one of the plurality of DSP units being inactive.

47. (New) The method of claim 43, wherein the selective stopping the clocking of respective plurality of DSP units is responsive to at least one of the plurality of DSP units not executing an instruction.

48. (New) The method of claim 43, wherein the selective activating one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.

49. (New) A method to conserve power in a digital

signal processor integrated circuit, the method comprising:

in an integrated circuit

selectively swapping activity between a reduced instruction set computing (RISC) processor and a plurality of digital signal processing (DSP) units, including activating and inactivating bus drivers on data paths in the RISC processor and the plurality of DSP units;

selectively stopping the clocking of at least one of the plurality of DSP units; and

selectively activating one of a plurality of memory clusters in an internal memory and maintaining a state of other memory clusters, including selecting a data flow path between the activated memory cluster and the RISC processor and the plurality of DSP units, the selected data flow path to change state while maintaining the state on data flow paths between inactivated memory clusters and the RISC processor and the plurality of DSP units..

50. (New) The method of claim 49, wherein

the selective stopping the clocking of at least one of the plurality of DSP units is responsive to at least one of the plurality of DSP units not executing an instruction.

51. (New) The method of claim 49, wherein

the selective activating one of the plurality of memory clusters in the internal memory is responsive to addressing a memory location within the respective one of the plurality of memory clusters.